



1109.001

Amendments

Please amend the above-identified U.S. application as follows:

In the Claims:

Please amend claims 1, 2, 4, 6, 15, 19, 23, 24, 56 & 58 as set forth below.

1. (Amended) A multichip module comprising:

a plurality of chips, each chip comprising an unpackaged chip having at least one side surface, an upper surface, a lower surface, and at least one contact pad at said upper surface;

a structural material surrounding and physically contacting the at least one side surface of each chip of said plurality of chips and mechanically interconnecting in spaced, planar relation said plurality of chips, said structural material having an upper surface substantially co-planar with an upper surface of each chip of said plurality of chips to form a first substantially co-planar surface, said first substantially co-planar surface comprising a front surface, and such that a lower surface of said structural material is substantially parallel with a lower surface of each chip of said plurality of chips to form a second surface, said second surface comprising a back surface; and

an in situ processed layer disposed on said front surface, said in situ processed layer comprising a material different from said structural material mechanically interconnecting said plurality of chips, said in situ

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23 processed layer including via openings to at least some  
24 contact pads at the upper surfaces of said plurality of  
25 chips for electrical connection thereto.

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1 ~~2~~. (Amended) [The multichip module of claim 1,] A  
2 multichip module comprising:

3 a plurality of chips, each chip comprising an  
4 unpackaged chip having at least one side surface, an upper  
5 surface, a lower surface, and at least one contact pad at  
6 said upper surface;

7 a structural material surrounding the at least one side  
8 surface of each chip of said plurality of chips and  
9 mechanically interconnecting in spaced, planar relation said  
10 plurality of chips, said structural material having an upper  
11 surface substantially co-planar with an upper surface of  
12 each chip of said plurality of chips to form a first  
13 substantially co-planar surface, said first substantially  
14 co-planar surface comprising a front surface, and such that  
15 a lower surface of said structural material is substantially  
16 parallel with a lower surface of each chip of said plurality  
17 of chips to form a second surface, said second surface  
18 comprising a back surface;

19 an in situ processed layer disposed on said front  
20 surface, said in situ processed layer comprising a material  
21 different from said structural material mechanically  
22 interconnecting said plurality of chips, said in situ  
23 processed layer including via openings to at least some  
24 contact pads at the upper surfaces of said plurality of  
25 chips for electrical connection thereto; and

26 wherein said structural material has a thickness equal  
27 to a thickest chip of said plurality of chips such that the

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28 upper surface of the structural material is substantially  
29 co-planar with the upper surface of the thickest chip to  
30 form said first substantially co-planar surface, and such  
31 that a lower surface of the structural material is  
32 substantially co-planar with a lower surface of said  
33 thickest chip of said plurality of chips to form a second  
34 substantially co-planar surface, said second substantially  
35 co-planar surface comprising said back surface.

1 <sup>17</sup> 4. (Amended) [The multichip module of claim 1,] A  
2 multichip module comprising:

3 a plurality of chips, each chip comprising an  
4 unpackaged chip having at least one side surface, an upper  
5 surface, a lower surface, and at least one contact pad at  
6 said upper surface;

7 a structural material surrounding the at least one side  
8 surface of each chip of said plurality of chips and  
9 mechanically interconnecting in spaced, planar relation said  
10 plurality of chips, said structural material having an upper  
11 surface substantially co-planar with an upper surface of  
12 each chip of said plurality of chips to form a first  
13 substantially co-planar surface, said first substantially  
14 co-planar surface comprising a front surface, and such that  
15 a lower surface of said structural material is substantially  
16 parallel with a lower surface of each chip of said plurality  
17 of chips to form a second surface, said second surface  
18 comprising a back surface;

19 an in situ processed layer disposed on said front  
20 surface, said in situ processed layer comprising a material  
21 different from said structural material mechanically  
22 interconnecting said plurality of chips, said in situ  
23 processed layer including via openings to at least some

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24 contact pads at the upper surfaces of said plurality of  
25 chips for electrical connection thereto; and

26 wherein each chip of said plurality of chips has a  
27 common thickness, and wherein said structural material  
28 surrounding and mechanically interconnecting said chips in  
29 spaced planar relation comprises a thickness equal to said  
30 common thickness of said plurality of chips such that said  
31 second surface comprises a second substantially co-planar  
32 surface wherein the lower surface of said structural  
33 material is substantially co-planar with the lower surface  
34 of each chip of said plurality of chips, and wherein said  
35 first substantially co-planar surface comprising said front  
36 surface is parallel to said second substantially co-planar  
37 surface comprising said back surface.

1 <sup>4</sup> ~~16~~. (Amended) The multichip module of claim <sup>3</sup> ~~5~~, wherein said  
2 multi-layer structure further comprises a release layer disposed  
3 over said in situ processed layer, said release layer being  
4 [thermally or chemically] removable without removing said in situ  
5 processed layer, said release layer comprising one of a  
6 thermoplastic material or a solventable material.

1 <sup>18</sup> ~~15~~. (Amended) [The multichip module of claim 14,] A  
2 multichip module comprising:

3 a plurality of chips, each chip comprising an  
4 unpackaged chip having at least one side surface, an upper  
5 surface, a lower surface, and at least one contact pad at  
6 said upper surface;

7 a structural material surrounding the at least one side  
8 surface of each chip of said plurality of chips and  
9 mechanically interconnecting in spaced, planar relation said  
10 plurality of chips, said structural material having an upper

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11 surface substantially co-planar with an upper surface of  
12 each chip of said plurality of chips to form a first  
13 substantially co-planar surface, said first substantially  
14 co-planar surface comprising a front surface, and such that  
15 a lower surface of said structural material is substantially  
16 parallel with a lower surface of each chip of said plurality  
17 of chips to form a second surface, said second surface  
18 comprising a back surface;

19 an in situ processed layer disposed on said front  
20 surface, said in situ processed layer comprising a material  
21 different from said structural material mechanically  
22 interconnecting said plurality of chips, said in situ  
23 processed layer including via openings to at least some  
24 contact pads at the upper surfaces of said plurality of  
25 chips for electrical connection thereto;

26 wherein each chip of said plurality of chips comprises  
27 a bare integrated circuit chip; and

28 wherein each chip of said plurality of chips has an  
29 equal thickness such that the upper surface of each chip is  
30 co-planar with said front surface and the lower surface of  
31 each chip is co-planar with said back surface, said back  
32 surface comprising a planar main surface of the multichip  
33 module.

1 <sup>20</sup>  
~~19.~~ (Amended) An integrated circuit chip module comprising:

2 an integrated circuit chip comprising a bare chip  
3 having a substrate, active circuitry associated with said  
4 substrate, an upper surface and a lower surface, said  
5 integrated circuit chip further comprising multiple  
6 electrical contact pads at said upper surface electrically  
7 coupled to said active circuitry, said integrated circuit

8 chip further having at least one side with a width defined  
9 by said upper surface and said lower surface;

10 a structural material surrounding and physically  
11 contacting said at least one side of said integrated circuit  
12 chip, said structural material having a top surface  
13 substantially co-planar with said upper surface of said  
14 integrated circuit chip to form a first surface, said first  
15 surface comprising a front surface, and said structural  
16 material having a bottom surface substantially parallel with  
17 said lower surface of said integrated circuit chip to form a  
18 second surface, said second surface comprising a back  
19 surface;

20 an in situ processed layer disposed on said front  
21 surface, said in situ processed layer comprising a material  
22 different from said structural material surrounding said at  
23 least one side of said integrated circuit chip, said in situ  
24 processed layer including at least one via opening to at  
25 least one contact pad of said multiple electrical contact  
26 pads at the upper surface of said integrated circuit chip;  
27 and

28 a metallization structure comprising metallization  
29 disposed within said at least one via opening electrically  
30 connecting to said at least one contact pad of said  
31 integrated circuit chip.

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1 25. (Amended) [The integrated circuit chip module of claim

2 20,] An integrated circuit chip module comprising:

3 an integrated circuit chip comprising a bare chip  
4 having a substrate, active circuitry associated with said  
5 substrate, an upper surface and a lower surface, said  
6 integrated circuit chip further comprising multiple

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7 electrical contact pads at said upper surface electrically  
8 coupled to said active circuitry, said integrated circuit  
9 chip further having at least one side with a width defined  
10 by said upper surface and said lower surface;

11 a structural material surrounding said at least one  
12 side of said integrated circuit chip, said structural  
13 material having a top surface substantially co-planar with  
14 said upper surface of said integrated circuit chip to form a  
15 first surface, said first surface comprising a front  
16 surface, and said structural material having a bottom  
17 surface substantially parallel with said lower surface of  
18 said integrated circuit chip to form a second surface, said  
19 second surface comprising a back surface;

20 an in situ processed layer disposed on said front  
21 surface, said in situ processed layer comprising a material  
22 different from said structural material surrounding said at  
23 least one side of said integrated circuit chip, said in situ  
24 processed layer including at least one via opening to at  
25 least one contact pad of said multiple electrical contact  
26 pads at the upper surface of said integrated circuit chip;

27 a metallization structure comprising metallization  
28 disposed within said at least one via opening electrically  
29 connecting to said at least one contact pad of said  
30 integrated circuit chip;

31 wherein said in situ processed layer comprises a photo-  
32 patternable dielectric material; and

33 wherein said bottom surface is substantially co-planar  
34 with said lower surface of said integrated circuit chip.

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24. (Amended) [The integrated circuit chip module of claim  
20,] An integrated circuit chip module comprising:

an integrated circuit chip comprising a bare chip  
having a substrate, active circuitry associated with said  
substrate, an upper surface and a lower surface, said  
integrated circuit chip further comprising multiple  
electrical contact pads at said upper surface electrically  
coupled to said active circuitry, said integrated circuit  
chip further having at least one side with a width defined  
by said upper surface and said lower surface;

a structural material surrounding said at least one  
side of said integrated circuit chip, said structural  
material having a top surface substantially co-planar with  
said upper surface of said integrated circuit chip to form a  
first surface, said first surface comprising a front  
surface, and said structural material having a bottom  
surface substantially parallel with said lower surface of  
said integrated circuit chip to form a second surface, said  
second surface comprising a back surface;

an in situ processed layer disposed on said front  
surface, said in situ processed layer comprising a material  
different from said structural material surrounding said at  
least one side of said integrated circuit chip, said in situ  
processed layer including at least one via opening to at  
least one contact pad of said multiple electrical contact  
pads at the upper surface of said integrated circuit chip;

a metallization structure comprising metallization  
disposed within said at least one via opening electrically  
connecting to said at least one contact pad of said  
integrated circuit chip;

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31 *ok* ✓ wherein said in situ processed layer comprises a photo-  
32 patternable dielectric material; and

33 wherein said back surface comprises an exposed planar  
34 main surface of said integrated circuit chip module.

1 <sup>27</sup>  
~~56~~. (Amended) A multichip module comprising:

2 a plurality of chips, each chip comprising an  
3 unpackaged chip having at least one side surface, an upper  
4 surface, and a lower surface; and

5 structural material surrounding and physically  
6 contacting the at least one side surface of each chip of  
7 said plurality of chips to mechanically interconnect in  
8 spaced planar relation said plurality of chips, said  
9 structural material having an upper surface co-planar with  
10 the upper surfaces of said plurality of chips, wherein a co-  
11 planar front surface is defined thereby, and wherein a lower  
12 surface of said structural material is substantially  
13 parallel with the lower surfaces of the plurality of chips,  
14 thereby defining a back surface.

1 <sup>29</sup>  
~~58~~. (Amended) [The multichip module of claim 56,] A  
2 multichip module comprising:

3 a plurality of chips, each chip comprising an  
4 unpackaged chip having at least one side surface, an upper  
5 surface, and a lower surface;

6 structural material surrounding the at least one side  
7 surface of each chip of said plurality of chips to  
8 mechanically interconnect in spaced planar relation said  
9 plurality of chips, said structural material having an upper  
10 surface co-planar with the upper surfaces of said plurality

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11 of chips, wherein a co-planar front surface is defined  
12 thereby, and wherein a lower surface of said structural  
13 material is substantially parallel with the lower surfaces  
14 of the plurality of chips, thereby defining a back surface;  
15 and

16 wherein the lower surface of the structural material is  
17 substantially co-planar with the lower surfaces of the  
18 plurality of chips.

Kindly add new claims 60 & 61 as follows:

1 ~~56~~. The multichip module of claim 1, wherein said  
2 structural material surrounds and physically contacts the at  
3 least one side surface of each chip so that there is no space  
4 between said structural material and said at least one side  
5 surface of each chip of said plurality of chips.--

1 ~~24~~. The integrated circuit chip module of claim 19,  
2 wherein said structural material surrounds and physically  
3 contacts the at least one side surface of said integrated circuit  
4 chip so that there is no space between said structural material  
5 and said at least one side surface of said integrated circuit  
6 chip.--

Remarks

Entry of this amendment, reconsideration of the application, and allowance of all claims pending herein are respectfully requested. By this amendment, claims 1, 6, 19 and 56 are amended and new claims 60 & 61 are added to more particularly point out and distinctly claim the subject matter of the present invention. Objected to claims 2, 4, 6, 15, 23, 24 & 58 are rewritten in independent form pursuant to the Examiner's suggestion in the first Office Action. Claims 1-24 & 56-61 are now pending. Of